

# Integrated Circuit Cooling Using Heterogeneous Micropin-Fin Arrays for Nonuniform Power Maps

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**Abstract**—As microelectronic system density continues to increase, cooling with conventional technologies continues to become more challenging and is often a limiter of performance and efficiency. The challenge arises due to both large heat fluxes generated across entire chips and packages, and localized hotspots with even higher heat flux. In this paper, nonuniform micropin-fin heat sinks are investigated for the cooling of integrated circuits with nonuniform power maps. Four heterogeneous micropin-fin samples were fabricated and tested in single-phase experiments with deionized water to investigate the effectiveness of local micropin-fin clustering for the cooling of hotspots. Cylindrical and hydrofoil micropin-fins were tested, as well as two types of heterogeneous arrays: those with pin-fins clustered directly over the hotspot and those with the high density cluster spanning the entire width of the channel to prevent flow bypass around the cluster. Samples were tested with a uniform nominal heat flux of 250 W/cm<sup>2</sup> as well as a hotspot heat flux of 500 W/cm<sup>2</sup>. Local micropin-fin clustering was found to be an effective method of reducing local thermal resistance with a modest pressure drop penalty.

**Index Terms**—Bosch process, deep reactive ion etching (DRIE), hotspot, microfluidic cooling, micropin-fin.

## I. INTRODUCTION

ONE major barrier to greater performance in modern integrated circuits (ICs) is the challenge of dissipating high heat fluxes and total package powers resulting from both traditional transistor scaling and high system integration density in the form of 2.5-D and 3-D systems. In addition to large average heat fluxes, localized hotspots with heat fluxes many times higher than the average chip heat flux may exist, ultimately setting the thermal envelope for the entire package [1]. Microfluidic cooling is an attractive approach to cooling these modern systems due to its ultralow junction-to-fluid thermal resistance, as well as its very small footprint and compatibility with high-density heterogeneous systems [2], [3].

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Microfluidic cooling was first demonstrated as a method of cooling high-power ICs in [4]. The thermal resistance from the active region to the fluid inlet in such a system can be described as follows:

$$R_{\text{tot}} = R_{\text{cond}} + R_{\text{conv}} + R_{\text{heat}} \quad (1)$$

where  $R_{\text{cond}}$  is the thermal resistance due to conduction through the silicon,  $R_{\text{conv}}$  is the thermal resistance associated with transferring the heat from the silicon to the fluid, and  $R_{\text{heat}}$  is the effective thermal resistance due to heating of the fluid. Since the demonstration in [4], several microfluidic heat sink geometries have been studied, including microchannels, cylindrical micropin-fins, and micropin-fins with several other cross-sectional shapes.

Prasher *et al.* [5] performed single-phase experiments on cylindrical silicon micropin-fin heat sinks with diameters between 50 and 150  $\mu\text{m}$  with water as a coolant. Correlations for friction factor and Nusselt number were developed to address the discrepancy between previously developed correlations and the observed experimental data. Koz and Kosar [6] and Tullius *et al.* [7] also performed parametric simulations of cylindrical micropin-fin arrays to study thermal and hydraulic performance as a function of micropin-fin design.

Brunschwiler *et al.* [8] investigated microchannels and micropin-fins with an emphasis on interlayer cooling in 3-D IC stacks. Inline and staggered micropin-fins were tested with different pitches in addition to micropin-fins with a teardrop shape. Single-phase thermal and hydraulic data were taken with water as a coolant and used to develop correlations for Nusselt number and friction factor as a function of micropin-fin geometry and flow conditions. Kosar and Peles [9] also reported thermal and hydraulic measurements on micropin-fin heat sinks with multiple cross-sectional shapes and reported the ideal shapes as a function of flow conditions. A number of studies have also looked at flow boiling with microchannels and micropin-fins [10], [11].

While previous work has focused primarily on characterizing uniform micropin-fin heat sinks, the diameter, transverse pitch, and longitudinal pitch of the micropin-fins can all be locally varied to create heterogeneous micropin-fin heat sinks. The ability to create heterogeneous microfluidic heat sinks with customizable local heat transfer coefficients is attractive for cooling systems in which power density is not uniform. By tailoring the heat sink design to the power map, temperature uniformity can be improved. Additionally, by only increasing micropin-fin density where needed, total pressure

drop can be minimized. In other words, pin-fin densities that may produce prohibitively high pressure drops when used over the entire chip can be used over a small area.

Several other methods of hotspot mitigation have been explored, including micro thermoelectric coolers (TECs) [12], liquid jet impingement [13]–[15], thin film evaporation [16], dedicated microgap coolers [10], [17], and heat spreading through highly thermally conductive materials, such as graphene [15], [18]. While all of these approaches have their advantages and disadvantages, they all require relatively complicated fabrication processes. Solutions such as TECs (and to some extent heat spreaders) can reduce temperatures of small hotspots, but still require a means of dissipating large background heat fluxes. The microfluidic heat sinks demonstrated in this paper are fabricated with a single etching step and are also compatible with TSVs and 3-D ICs [19].

Green *et al.* [20] used a 3-D strip model in ANSYS FLUENT to investigate the effect of micropin-fin clustering for hotspot cooling. A local doubling of pin-fin density was found to reduce local thermal resistance by a factor of roughly two. The strip model included symmetry constraints on either side, effectively simulating an infinite array of identical “cooling strips,” with a high-density pin-fin cluster spanning that entire channel. More recently, Lorenzini *et al.* [21] performed full-chip flow and heat transfer simulations with cylindrical micropin-fins, showing effective hotspot cooling with locally clustered micropin-fins.

Heterogeneous micropin-fin arrays are used in this paper to cool a uniform background heat flux with a higher heat flux, hotspot region. Since flow could be diverted around a high-density pin-fin cluster not spanning the entire width of the channel, two types of clusters were chosen for experimental investigation: local clustering over the hotspot and clustering spanning the entire width of the channel. Pin-fins with both circular and hydrofoil shaped cross sections were also tested.

This paper is organized as follows. First, an analysis of the effect of lateral heat spreading through the base of the heat sink is presented. Then, fabrication results are shown for micropin-fin arrays fabricated with a wide range of dimensions on a single wafer. Next, a thermal testbed and the four test chips with heterogeneous micropin-fin arrays are described. Finally, thermal measurements of the four different micropin-fin test chips are presented and analyzed.

## II. EFFECT OF HEAT SPREADING

Even with a uniform micropin-fin array, heat spreading through the silicon bulk will act to partially mitigate hotspots. In order to quantify the effect of spreading as a function of base thickness and the ratio of hotspot heat flux to background heat flux, heat transfer simulations were performed with COMSOL 4.3b. A 3-D model of a 1-cm×1-cm chip was created with a 500- $\mu\text{m}$ ×500- $\mu\text{m}$  hotspot region in the center. Symmetry boundary conditions were utilized to only simulate a quarter of this geometry. A maximum mesh size of 10  $\mu\text{m}$  was used in the region over the hotspot, and a maximum mesh size of 50  $\mu\text{m}$  was used over the background region, with a maximum growth rate of 1.1 between the two regions.

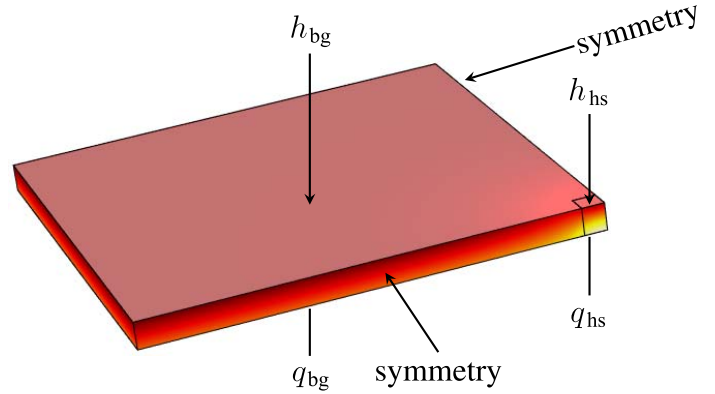


Fig. 1. COMSOL heat spreading model.

On the bottom of the chip slice, two heat fluxes were applied, one to the hotspot ( $q_{hs}$ ) and one to the background region ( $q_{bg}$ ). On the top side of the chip, two heat transfer coefficients were applied, one over the hotspot region ( $h_{hs}$ ), and another over the remaining background region ( $h_{bg}$ ). An illustration of the model can be seen in Fig. 1. The reference temperature on the convective boundary conditions,  $h_{hs}$  and  $h_{bg}$ , was set to a constant 20 °C. Although a microfluidic heat sink would have a gradient in this boundary temperature due to heating of the fluid, using a linear temperature gradient across the chip does not affect the average temperatures in the simulations. The hotspot heat flux can locally heat the fluid, but this effect is expected to be small since the hotspot area is 0.25% of the total chip area. Therefore, the hotspot power is a small fraction of the total power, even when the hotspot heat flux density is several times the average heat flux density.

### A. Effect of Base Thickness on Hotspot Temperature

In the first parametric study, the effect of base thickness on hotspot temperature was measured for a silicon thickness range of 0 to 500  $\mu\text{m}$ . The background heat flux was set to 250 W/cm<sup>2</sup>, while the hotspot heat flux was set to 500 W/cm<sup>2</sup>. The background and hotspot heat transfer coefficients were both set to 100 000 W/(°C m<sup>2</sup>), representing a uniform micropin-fin array. Fig. 2 shows the average background and hotspot temperature rise above ambient as a function of base thickness.

The background temperature rise above ambient is approximately a linear function of base thickness due to the conductive thermal resistance of the silicon. The hotspot temperature, on the other hand, initially decreases with increasing silicon base thickness due to lateral heat spreading through the silicon. Spreading then rapidly tapers off with increasing silicon base thickness, and the hotspot temperature reaches a minimum at a thickness of approximately 130  $\mu\text{m}$ . The hotspot temperature then increases with increasing thickness due to the increasing conductive thermal resistance of the silicon.

The hotspot temperature can also be influenced by changing the local heat transfer coefficient over the hotspot. Fig. 3 shows the average hotspot and background temperatures when the hotspot heat transfer coefficient is  $1 \times h_{bg}$ ,  $2 \times h_{bg}$ , and  $5 \times h_{bg}$ . The average background temperatures are relatively unaffected

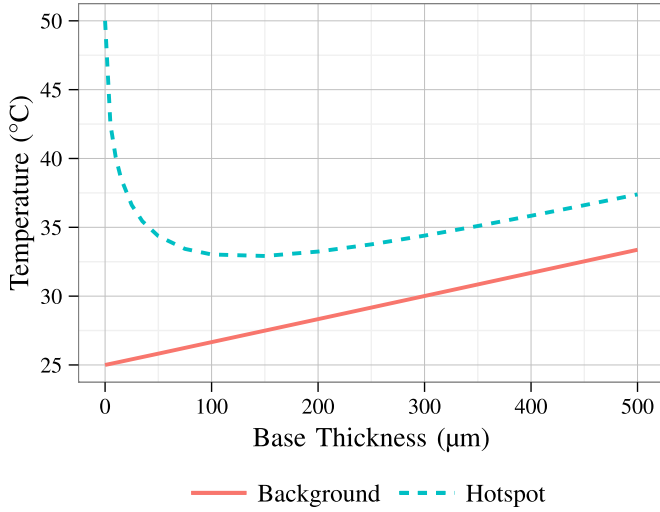


Fig. 2. Simulated surface averaged hotspot and background temperature rise above ambient versus silicon base thickness with uniform heat transfer coefficient [ $100\,000\text{ W}/(\text{m}^2\text{ }^\circ\text{C})$ ], hotspot heat flux of  $500\text{ W}/\text{cm}^2$ , and background heat flux of  $250\text{ W}/\text{cm}^2$ .

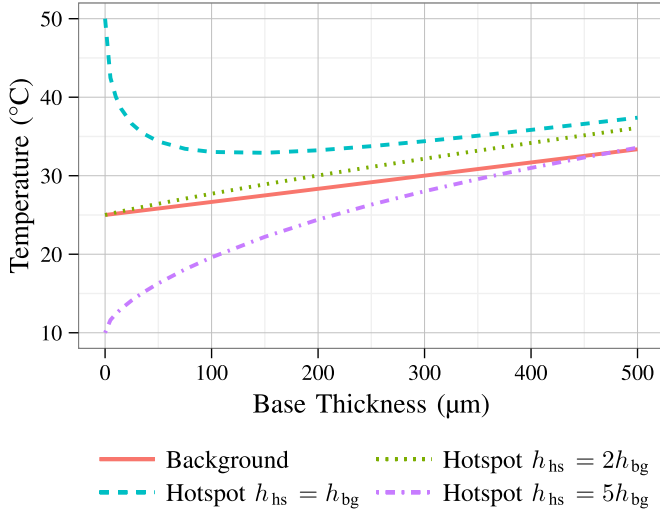


Fig. 3. Simulated surface averaged hotspot and background temperature rise above ambient versus silicon base thickness with a hotspot heat flux of  $500\text{ W}/\text{cm}^2$ , a background heat flux of  $250\text{ W}/\text{cm}^2$ , a background heat transfer coefficient ( $h_{bg}$ ) of  $100\,000\text{ W}/(\text{m}^2\text{ }^\circ\text{C})$ , and hotspot heat transfer coefficients of  $1 \times h_{bg}$ ,  $2 \times h_{bg}$ , and  $5 \times h_{bg}$ .

by the much smaller hotspot conditions, only varying by less than 0.3% between these three cases, so they are drawn as a single line, averaging the three cases. While heat spreading through the base can decrease hotspot temperature with uniform cooling, spreading increases the temperature in the cases with enhanced cooling over the hotspot shown in Fig. 3.

### B. Measuring Thermal Resistance at the Hotspot

Without heat spreading through the base silicon, one could characterize the heterogeneous heat sink by calculating separate background and hotspot thermal resistances (at specific flow conditions). However, when we define the hotspot thermal resistance as  $R_{hs} = (T_{hs} - T_{amb})/q_{hs}$ , where  $T_{hs}$  is the average

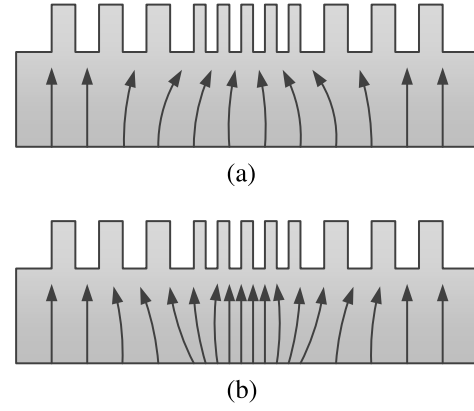


Fig. 4. Direction of heat flow in the substrate for different power maps. (a) Uniform heat flux. (b) High hotspot heat flux.

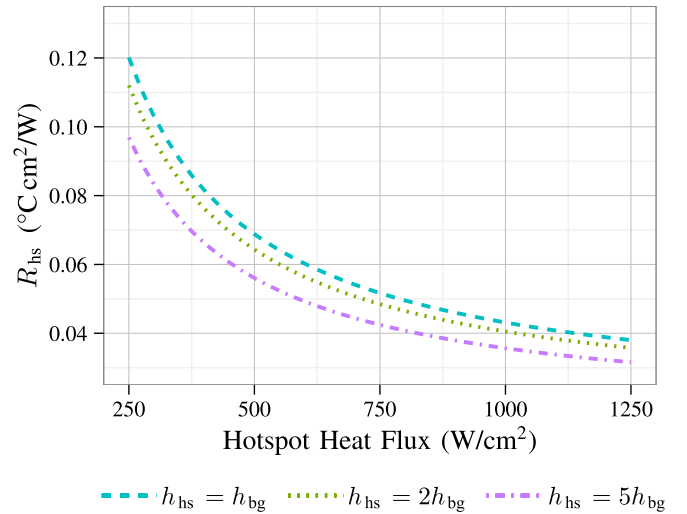


Fig. 5. Effective hotspot thermal resistance ( $R_{hs}$ ) versus hotspot heat flux ( $q_{hs}$ ).

hotspot temperature and  $T_{amb}$  is the reference temperature on the convective boundary condition, the apparent thermal resistance at the hotspot (and to a much lesser extent, the background region) depends on the power map applied. When a uniform power map is applied, some heat from the background region is transferred to the high-density cluster, making the apparent thermal resistance greater than it would be with no spreading (with a very thin base). However, as local heat flux increases, heat begins to leave the dense cluster and finds another path by spreading through the base, causing the apparent thermal resistance to decrease. This effect is illustrated in Fig. 4.

The effective thermal resistance at the hotspot,  $R_{hs}$ , is shown in Fig. 5 where the silicon base thickness is  $300\text{ }\mu\text{m}$  and the background heat flux is  $250\text{ W}/\text{cm}^2$ . Three lines are shown, where  $h_{hs} = 100\,000\text{ W}/(\text{m}^2\text{ }^\circ\text{C})$ ,  $h_{hs} = 200\,000\text{ W}/(\text{m}^2\text{ }^\circ\text{C})$ , and  $h_{hs} = 500\,000\text{ W}/(\text{m}^2\text{ }^\circ\text{C})$ . Due to heat spreading to the surrounding background region, the apparent hotspot thermal resistance changes with hotspot heat flux. Therefore, in Section IV, hotspot performance will be reported as temperatures relative to background temperatures.

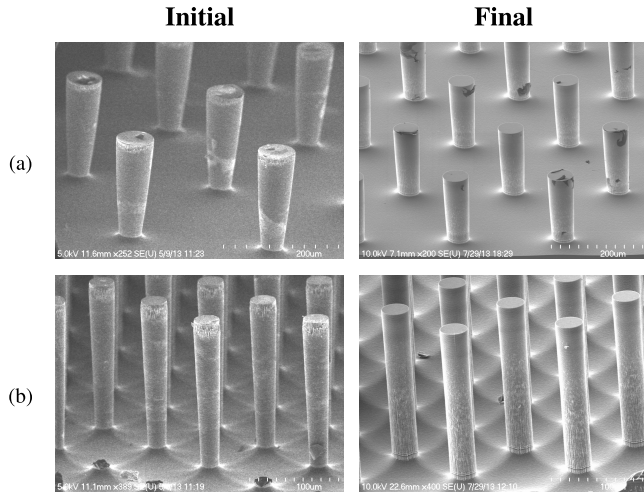


Fig. 6. SEM images of (a) sparse and (b) dense, high-aspect-ratio micropin-fins before and after etching process optimization.

### III. FABRICATION OF MULTIPLE MICROPIN-FIN DENSITIES ON A SINGLE WAFER

In order to locally tailor heat transfer to the fluid, micropin-fins of varying dimensions must be built on the same wafer and, ideally, in the same processing steps. The micropin-fins used in this paper were etched into silicon using the Bosch process and an STS inductively coupled plasma machine. The process consists of a reactive ion etching step with an  $\text{SF}_6$  plasma, followed by a passivation step with  $\text{C}_4\text{F}_8$ . RF power is applied to the wafer platen in order to create a bias that accelerates ions toward the wafer.

In order to produce heterogeneous micropin-fin arrays, the Bosch process used for etching had to be optimized in order to produce reasonable results for all dimensions with a single wafer-level batch process. This is particularly challenging for high-aspect-ratio micropin-fins, which can be desirable from a thermal perspective for their large surface area. While ideal etching conditions vary between very dense and sparse micropin-fin arrays, a recipe was developed that produced acceptable results for both.

As seen in Fig. 6, the largest issue was micropin-fin sidewall tapering on very sparse micropin-fin arrays. Significant tapering could decrease fin efficiency and produce results that deviate from expected results with cylindrical micropin-fins. This was improved by increasing the ratio of passivation time to etching time. Platen power was increased during the etch step, and the total cycle time was increased relative to the default trench etching recipe, yielding the final etching recipe consisting of a 14-s etch step, a 17.5-s passivation step, and a platen power of 20 W. This recipe was used to produce the results shown in Fig. 7, which shows sidewall profiles of six different micropin-fin arrays built on a single wafer. Dense, sparse, and high-aspect-ratio dimensions are included and can be seen in Table I. Heat transfer and pressure drop studies were carried out with these samples in [22]. Four of the micropin-fin arrays have a micropin-fin diameter of  $30\text{ }\mu\text{m}$ , which is substantially smaller than the majority of micropin-fins studied in literature. Since all micropin-fins were etched to a nominal

TABLE I  
CYLINDRICAL MICROPIN-FIN DIMENSIONS BUILT ON A SINGLE WAFER

Die Number	Diameter	Transverse Pitch	Lateral Pitch
Die 1	$30\text{ }\mu\text{m}$	$90\text{ }\mu\text{m}$	$90\text{ }\mu\text{m}$
Die 2	$60\text{ }\mu\text{m}$	$240\text{ }\mu\text{m}$	$240\text{ }\mu\text{m}$
Die 3	$120\text{ }\mu\text{m}$	$420\text{ }\mu\text{m}$	$180\text{ }\mu\text{m}$
Die 4	$30\text{ }\mu\text{m}$	$90\text{ }\mu\text{m}$	$30\text{ }\mu\text{m}$
Die 5	$30\text{ }\mu\text{m}$	$75\text{ }\mu\text{m}$	$36\text{ }\mu\text{m}$
Die 6	$30\text{ }\mu\text{m}$	$120\text{ }\mu\text{m}$	$60\text{ }\mu\text{m}$

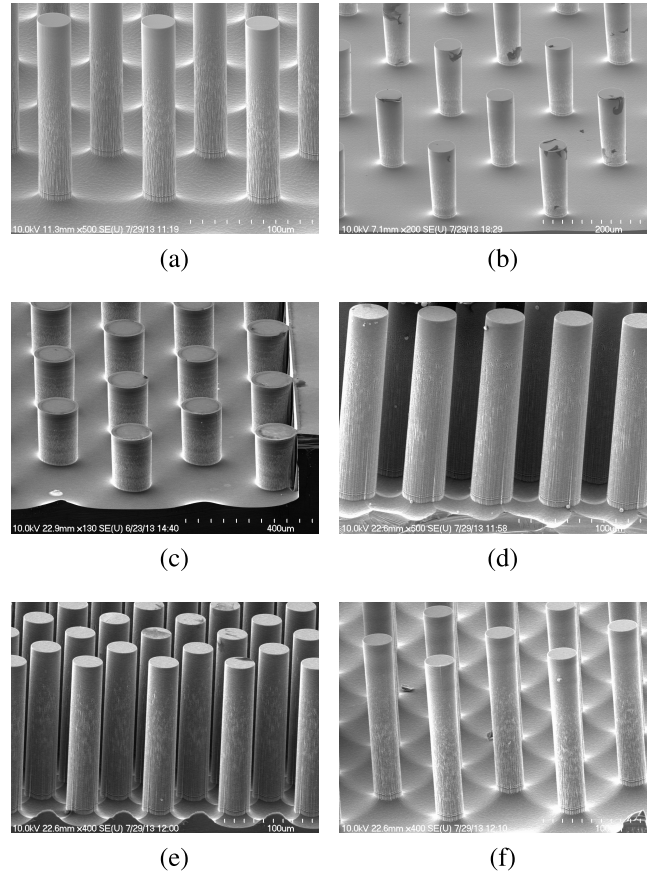


Fig. 7. Six micropin-fin dice etched using a single-batch process on the same wafer. (a) Die 1. (b) Die 2. (c) Die 3. (d) Die 4. (e) Die 5. (f) Die 6.

height of  $200\text{ }\mu\text{m}$ , these small diameter micropin-fins have an aspect ratio of 6.7:1, which is also necessary for high surface area enhancement, but makes sidewall profile crucial.

### IV. THERMAL TESTBED AND HETEROGENEOUS MICROPIN-FIN SAMPLES

In this paper, chip heat flux is represented by a “background” heat flux and a “hotspot” heat flux. The hotspot is a smaller region of the chip, with a heat flux considerably higher than that of the background region. By locally clustering micropin-fins over a hotspot, it is expected that the local heat transfer coefficient can be increased to deal with the hotspot heat fluxes, while minimizing the pressure drop penalty compared to using this high-density clustering over the entire background region.



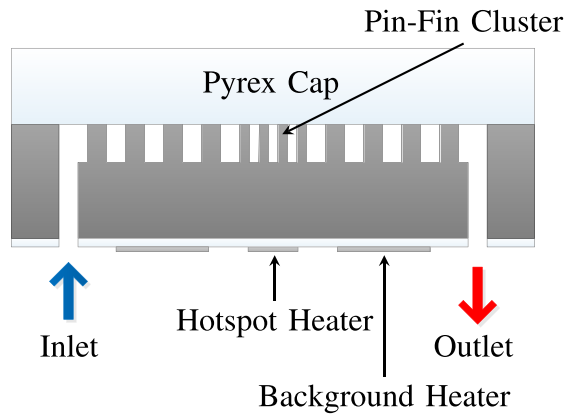


Fig. 8. Heterogeneous micropin-fin test chip cross section.

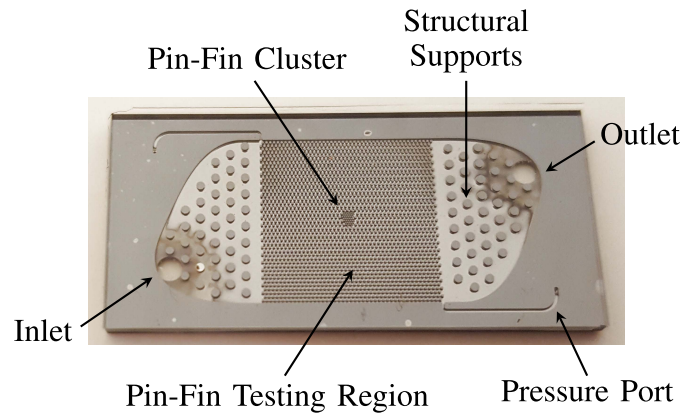
The etching recipe discussed above was applied to heterogeneous micropin-fin arrays with local clustering of micropin-fins over hotspots. First, the micropin-fins were etched into a  $500\text{-}\mu\text{m}$  double-side polished silicon wafer. A pyrex cap was anodically bonded to the micropin-fins to seal the channels. Next, a  $1.9\text{-}\mu\text{m}$ -thick silicon dioxide layer was deposited on the back side of the wafer, on top of which  $0.2\text{-}\mu\text{m}$ -thick platinum heaters were deposited. The heaters also acted as resistance temperature detectors (RTDs). Finally, fluid inlet/outlet and pressure measurement ports were etched through the silicon. A cross-sectional diagram of the test chips can be seen in Fig. 8.

While enhanced heat transfer is only necessary over the hotspot, local clustering over this region is expected to result in some flow diversion around the higher density clustering. Therefore, for both the hydrofoil and circular micropin-fin designs, clustering was done in a small region over the hotspot as well as in a region spanning the entire width of the channel to prevent this flow diversion. Four different background/hotspot test devices were fabricated, with two types of micropin-fin cross-sectional shapes and two types of clustering for hotspot cooling as follows:

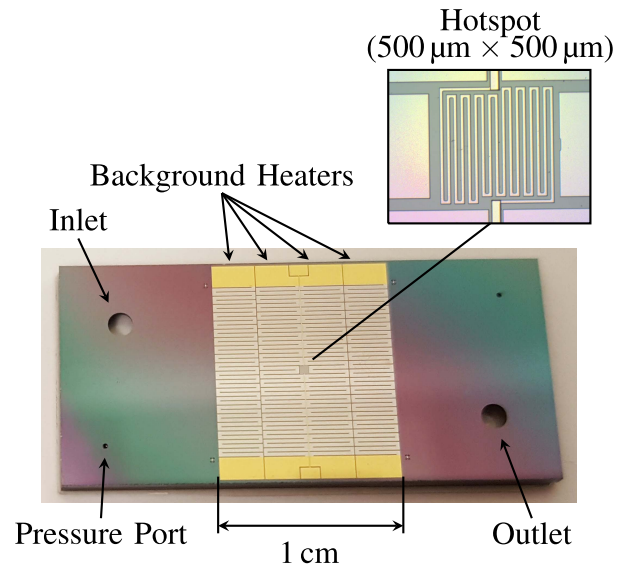
- 1) cylindrical micropin-fins with local clustering;
- 2) cylindrical micropin-fins with span-wise clustering;
- 3) hydrofoil micropin-fins with local clustering;
- 4) hydrofoil micropin-fins with span-wise clustering.

Images of the top and bottom of a micropin-fin test device can be seen in Fig. 9. The background micropin-fin array covers an area of  $1\text{ cm} \times 1\text{ cm}$ . The hotspot consists of an area of  $500\text{ }\mu\text{m} \times 500\text{ }\mu\text{m}$  in the center of the chip. This region is heated by a dedicated serpentine platinum heater on the bottom of the chip while background heat flux is applied through four heaters spanning the chip. Pressure ports at the inlet and outlet sides of the background micropin-fin array provide accurate pressure drop measurements.

Dimensions of the background micropin-fins can be seen in Fig. 10. The diameter of the cylindrical micropin-fins is  $150\text{ }\mu\text{m}$ . The transverse and longitudinal pitches are both  $225\text{ }\mu\text{m}$ . The width of the background hydrofoil micropin-fins is  $150\text{ }\mu\text{m}$ , and the transverse and longitudinal pitches are  $225$  and  $642.5\text{ }\mu\text{m}$ , respectively. All micropin-fins were



(a) Top side of die with micropin-fins



(b) Bottom side of die with heaters and fluid ports

Fig. 9. Test chip. (a) Top view of etched silicon through pyrex cap. (b) Bottom view of heaters and ports.

etched to a nominal height of  $200\text{ }\mu\text{m}$ . Pitches and diameters of micropin-fins in the high-density clusters were half of the background pitches and diameters. SEM images of the micropin-fin clustering over the hotspots for the four different heat sinks can be seen in Figs. 11–14.

Each chip was tested in an open-loop system with deionized water as a coolant, with an inlet temperature of  $21 \pm 0.5\text{ }^\circ\text{C}$ . A diagram of the open flow loop can be seen in Fig. 15. RTD resistance versus temperature calibration lines were first generated by measuring RTD resistances at temperatures ranging from approximately  $20\text{ }^\circ\text{C}$  to approximately  $110\text{ }^\circ\text{C}$ . The chips were placed in a package with O-ring seals on the ports for fluid delivery and pressure measurement. Fluid temperature was measured at the inlet and outlet of the package with k-type thermocouples calibrated to an accuracy of  $0.1\text{ }^\circ\text{C}$  over the range of temperatures used in experimentation. Flow rate was measured with a rotameter with a maximum uncertainty of less than  $2\text{ mL/min}$ . Pressure drop across the micropin-fin arrays was measured using a digital differential pressure gauge

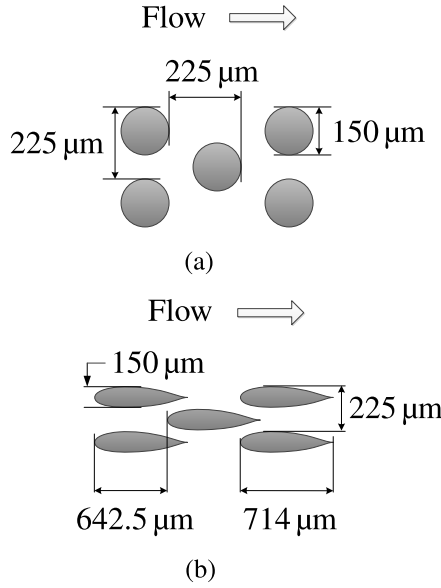


Fig. 10. Background micropin-fin dimensions. (a) Background circular micropin-fin dimensions. (b) Background hydrofoil micropin-fin dimensions.

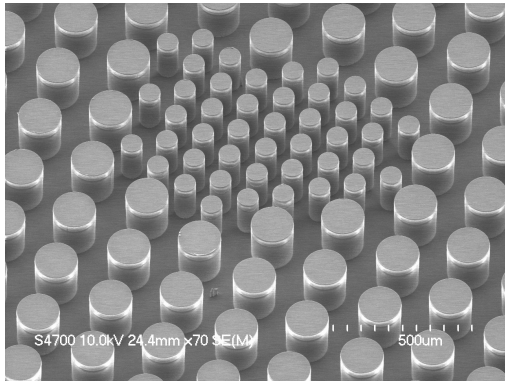


Fig. 11. Cylindrical micropin-fins locally clustered over hotspot.

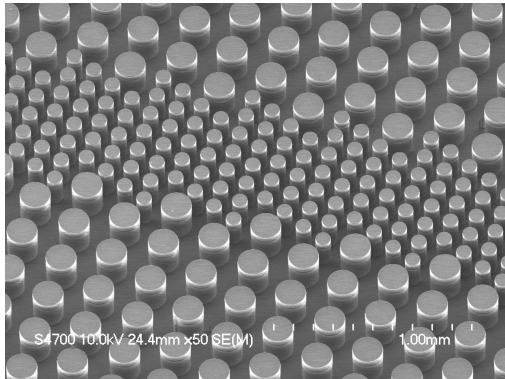


Fig. 12. Cylindrical micropin-fins spanning entire channel.

calibrated with an Omega DPI610 calibrator to within 0.1 kPa. RTD power and resistance were recorded with an Agilent data logger.

Each experiment was run twice, and the averages of the results from the two runs are reported in Section V. In order to

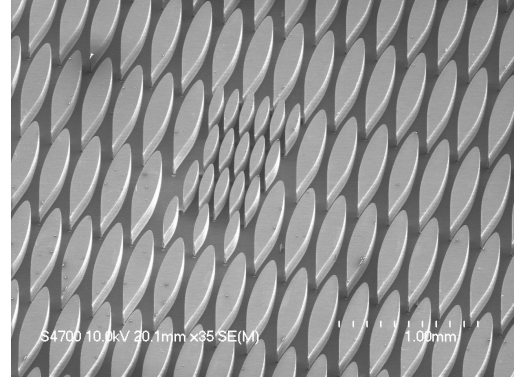


Fig. 13. Hydrofoil micropin-fins locally clustered over hotspot.

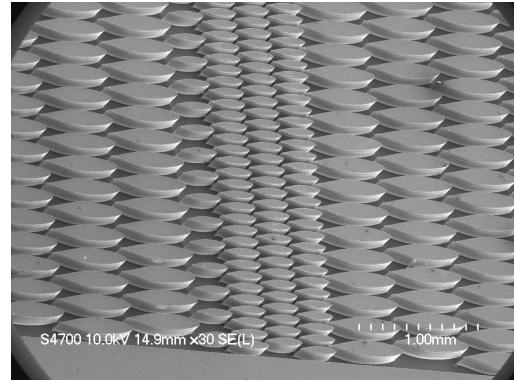


Fig. 14. Hydrofoil micropin-fins spanning entire channel.

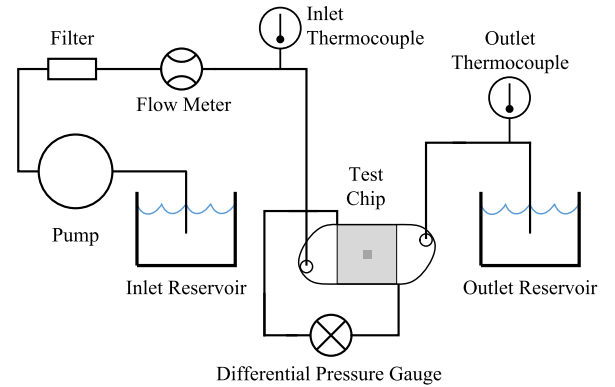


Fig. 15. Diagram of open loop system used to test chips.

quantify the uncertainty in the RTD temperature measurements as well as the pressure measurements, combined standard deviations across these repeated runs were calculated and are reported in Table II along with the measurement device uncertainties.

The amount of heat lost to the ambient surroundings can be calculated from measured quantities according to

$$Q_{\text{loss}} = Q_{\text{in}} - \dot{m}C_p(T_{\text{out}} - T_{\text{in}}) \quad (2)$$

where  $\dot{m}$  is the water mass flow rate,  $C_p$  is the specific heat of water (approximately 4.18 J/(g°C)), and  $T_{\text{in}}$  and  $T_{\text{out}}$  are the measured water inlet and outlet temperatures, respectively.

TABLE II  
MEASUREMENT UNCERTAINTIES

Pressure Gauge Accuracy	0.1 kPa
Thermocouple Measurement Accuracy	0.1 °C
Flow Rate Measurement Accuracy	2 mL/min
Combined Temperature Standard Deviation	0.33 °C
Combined Pressure Standard Deviation	1.3 kPa

Heat loss to ambient was found to be below 3.35% for all data points.

Due to the high heat fluxes and low convective thermal resistances in these experiments, temperature drop across the 1.9- $\mu\text{m}$ -thick silicon dioxide insulation under the platinum heaters accounted for a substantial portion of the temperature difference between the RTDs and the fluid. This temperature drop across the silicon dioxide layer was estimated through heat conduction simulations in COMSOL, taking the thermal conductivity of PECVD silicon dioxide to be 1.1 W/(m °C) [23], [24]. Since the serpentine heaters do not provide completely uniform heat flux, the temperature drop across the silicon dioxide is higher than 1-D conduction calculations would predict. The temperature drop from the RTD to the silicon was found to be 7.9 °C and 15.8 °C for nominal hotspot heat fluxes of 250 and 500 W/cm<sup>2</sup>, respectively. From the background RTDs to the silicon, this number was 5.2 °C at 250 W/cm<sup>2</sup>. These numbers were used to compute the temperatures at the silicon surface, called the junction temperature, or  $T_j$ .

## V. EXPERIMENTAL RESULTS

Fig. 16 shows junction temperature rise above inlet temperature ( $T_j - T_{in}$ ) versus axial position in the direction of fluid flow ( $x$ ) for all four types of chips at a flow rate of 208 mL/min and a uniform power of 246 W across the 1-cm $\times$ 1-cm chips. Maximum variation in heat flux between the four heaters was found to be between 1% and 4%. With a uniform micropin-fin array, uniform power, constant fluid heat capacity, and no edge effects, one would expect the junction temperature to increase linearly with axial position. A line was fit to the four background junction temperatures using least squares. As can be seen, the temperature does rise linearly, although the first and last temperatures tend to be below the fit line, while the center heaters tend to be above. This could be a result of heat spreading to the inlet and outlet plena as well as flow development in these regions.

The slopes of the lines in Fig. 16 have units of °C/mm and depend primarily on flow rate and heat flux rather than the micropin-fin dimensions. As expected, all four lines have the same slope. By multiplying the slope by the length of the chip, the change in fluid temperature across the 1-cm length of the micropin-fin region can be estimated. Since this gradient across the micropin-fin region of the chip only accounts for approximately 85% of the measured  $T_{out} - T_{in}$ , it is estimated that approximately 15% of the heat flux was spread to the inlet and outlet plena where it was transferred to the water.

As can be seen, the background  $T_j$  values for all four chips are very similar. A larger difference can be seen in the hotspot temperatures. Since the hotspots have the same power density

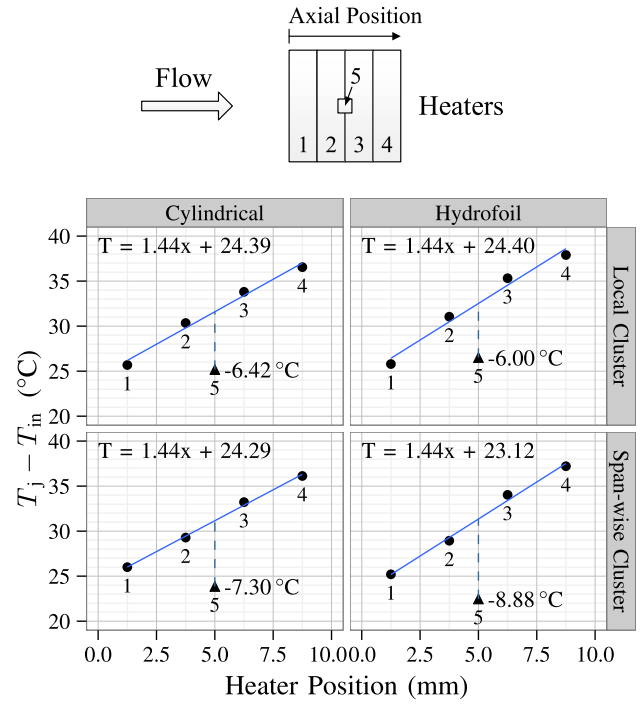


Fig. 16. Junction temperature rise above inlet temperature versus axial position in the direction of fluid flow with a uniform 246-W power. Hotspot labels represent temperature deviation from expected temperature with a uniform micropin-fin density.

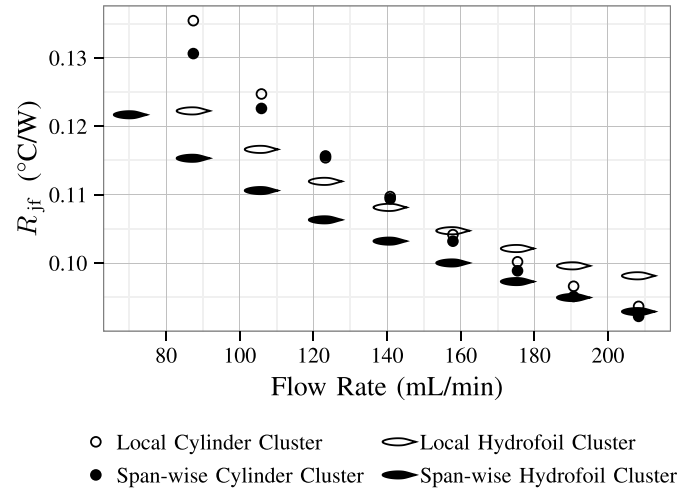


Fig. 17. Thermal resistance from the silicon to fluid ( $R_{jf}$ ) versus flow rate for all four dice.

as the rest of the chip for this data set, the temperature would be expected to fall on the best-fit line with uniform micropin-fins. The hotspot temperature deviation from the line is shown on each plot and illustrates the performance improvement from the high-density clustering. All four designs offered a performance improvement through clustering, but the hydrofoil cluster spanning the entire width of the chip performed best, reducing temperature by 8.88 °C versus the background.

The average background junction-to-fluid thermal resistance,  $R_{jf} = R_{cond} + R_{conv}$ , can be found by subtracting the average fluid temperature from the average junction temperature and dividing by the chip power. Fig. 17 shows background



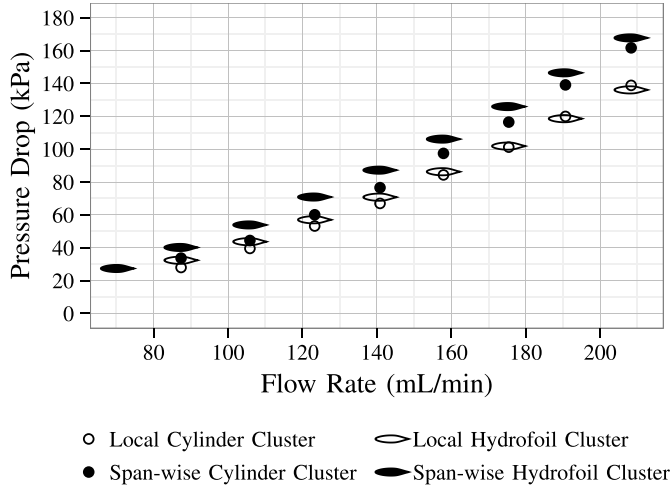


Fig. 18. Pressure drop versus flow rate for all four dice.

$R_{jf}$  versus flow rate for all four test chips. It should be noted that this includes any effects of the higher density micropin-fin cluster on the background measurements, which can be significant for the micropin-fins spanning the width of the channel, as they cover a larger surface area and are located directly above sections of the background RTDs. Therefore, it is unsurprising that the average background thermal resistance of the hydrofoil sample with span-wise clustering is lower than that of the hydrofoil sample with local clustering, despite the same dimensions of micropin-fins over the rest of the sample.

Pressure drop versus flow rate for the four dice can be seen in Fig. 18. The four samples have very similar pressure drops, but, unsurprisingly, the two samples with the high-density clustering spanning the width of the channel have the highest pressure drops. The hydrofoil sample with span-wise clustering had the lowest background and hotspot temperatures, but also had the highest pressure drop.

The Reynolds number was calculated for all four dice. With the characteristic length defined as the hydraulic diameter of the gap between micropin-fins, the Reynolds number ranges from a minimum of 190.5, at the lowest flow rate, to a maximum of 873, at the highest flow rate. Beyond a Reynolds number around 100–300, a flow transition leading to higher pressure drops has previously been observed in micropin-fin arrays [5], [8]. This transition was shown by Renfer *et al.* [25] to occur when the flow transitions from steady laminar flow to a regime with vortex shedding. Since most of the Reynolds numbers in this paper were close to or above this range for all of the flow rates and chips tested, the flow was likely to be in this flow regime with vortex shedding.

#### A. Nonuniform Heat Flux

Lastly, all four devices were tested with a nominal background heat flux of  $250 \text{ W/cm}^2$  and a hotspot heat flux of  $500 \text{ W/cm}^2$ . Results at the highest flow rate of  $208 \text{ mL/min}$  can be seen in Fig. 19. Despite doubling the heat flux relative to the background region, hotspot temperatures remain below the background centerline temperatures.

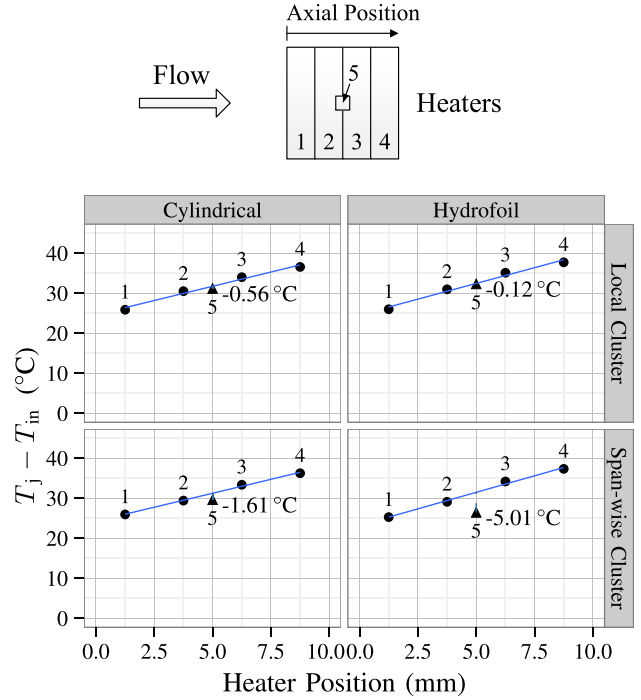


Fig. 19. Junction temperature rise above inlet temperature versus axial position in the direction of fluid flow with  $500 \text{ W/cm}^2$  hotspot heat flux and  $250 \text{ W/cm}^2$  background heat flux. Hotspot labels represent temperature deviation from expected temperature with a uniform micropin-fin density.

Background and hotspot temperatures are shown for all four devices as a function of flow rate in Fig. 20. Hotspot junction temperature rise above inlet temperature is shown for nominal hotspot heat fluxes of  $250$  and  $500 \text{ W/cm}^2$  with a background heat flux of  $250 \text{ W/cm}^2$ . The average background temperature across all four background heaters is also shown. Since the total hotspot power was much lower than the background power (due to its smaller size), the average background temperature was minimally affected by the hotspot heat flux. Therefore, a single set of background temperature points is shown, representing the average background temperatures between the experiments with the two hotspot heat fluxes. Each of these average background temperature values varies by less than  $0.5\%$  from the measured temperatures in either of the experiments.

As can be seen in Fig. 20, the hotspot temperature is lower than the average background temperature for all uniform power maps ( $250 \text{ W/cm}^2$  background and hotspot). When the hotspot heat flux is increased to  $500 \text{ W/cm}^2$ , the hotspot temperature increases, but remains below average background temperature for most of the four device types. The hydrofoil micropin-fins with local clustering have a hotspot temperature that matches the background temperature very closely when the hotspot heat flux is twice the background heat flux (maximum difference of  $0.25^\circ\text{C}$ , or  $0.4\%$ ). As seen before, the hydrofoil device with high-density micropin-fins spanning the entire width of the channel has the lowest hotspot temperatures and would likely be ideal for even higher hotspot heat fluxes relative to background heat fluxes.

The two devices with micropin-fins spanning the entire width of the channel had lower hotspot temperatures than

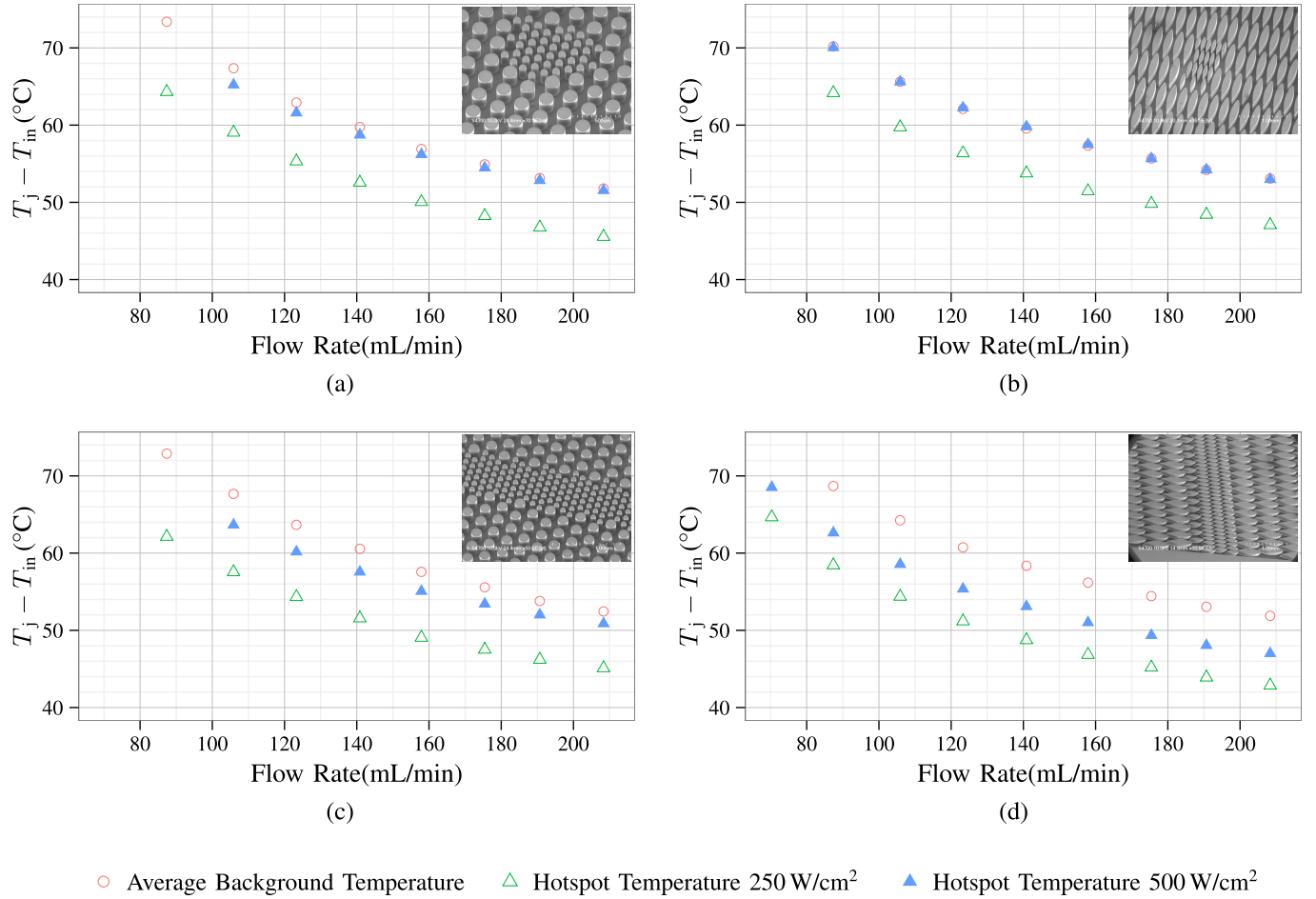


Fig. 20. Hotspot and background temperatures versus flow rate of all four chips. (a) Cylindrical micropin-fins with local clustering. (b) Hydrofoil micropin-fins with local clustering. (c) Cylindrical micropin-fins with span-wise clustering. (d) Hydrofoil micropin-fins with span-wise clustering.

those with clustering directly over the hotspot. This could be partially due to flow diversion around the cluster when the cluster does not span the entire width of the channel, but also because of heat spreading to the larger high-density cluster when the cluster extends beyond the hotspot region.

## VI. CONCLUSION

In this paper, heterogeneous micropin-fin arrays were fabricated and tested for the cooling of ICs with hotspots. Two types of micropin-fins (cylindrical and hydrofoil) were tested, each with clustering directly over the hotspot, and clustering spanning the entire width of the channel to prevent flow bypass (a total of four devices).

Of the four devices, the device with the hydrofoil shaped micropin-fins and the dense cluster spanning the entire width of the channel had the lowest hotspot temperatures and the lowest background temperatures at many of the flow rates tested. With a uniform power map and the highest flow rate of 208 mL/min, this sample had a background junction-to-fluid thermal resistance of 0.093 °C cm²/W.

All four devices effectively reduced hotspot temperatures. With a nominal hotspot heat flux of 500 W/cm² and a nominal background heat flux of 250 W/cm², the average

junction temperatures between the hotspot and background were matched very closely for all flow rates on both the samples with only local clustering directly over the hotspot. Background and hotspot average temperatures, relative to inlet temperature, differed by a maximum of 0.4% for all flow rates with the hydrofoil device.

The two devices with micropin-fins spanning the entire width of the channel had lower hotspot temperatures than those with local clustering, at the cost of higher pressure drop. This difference in hotspot thermal performance may partially result from flow diversion around the local clusters, but also likely arises from heat spreading to areas of the high-density clusters that are not directly above the hotspot.

Heat spreading to larger clustered areas could be utilized in future work with higher density clusters extending beyond the limits of the hotspot in both dimensions. In this paper, average background and hotspot temperatures were used, but more detailed temperature maps could also be investigated to resolve the boundaries between these regions and mitigate maximum temperatures. In fact, continuously varying micropin-fin pitches could also be utilized, potentially eliminating almost all temperature variation across the chip for a given power map.



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